Title: "Methodology For Performing Registered Read/Write To Two Or More Expanders With A Common Test Port"
Inventors: Gabriel L. Romero & Jeffrey Gauvin Docket Number: LSI.87US01(03-0760)
Attorney: William W. Cochran Registration #: 26,652 Phone: 970.377.6363

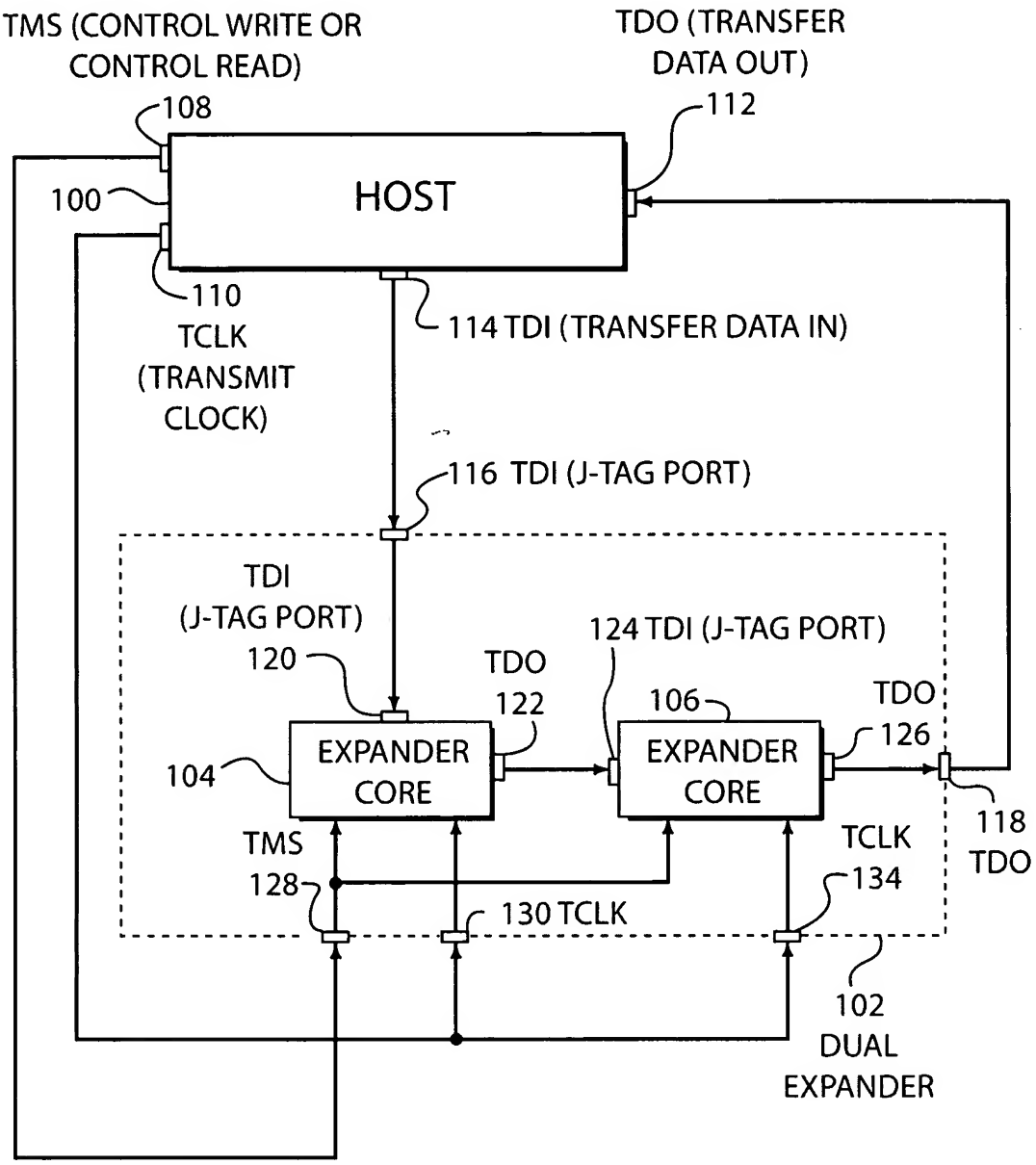

FIGURE 1

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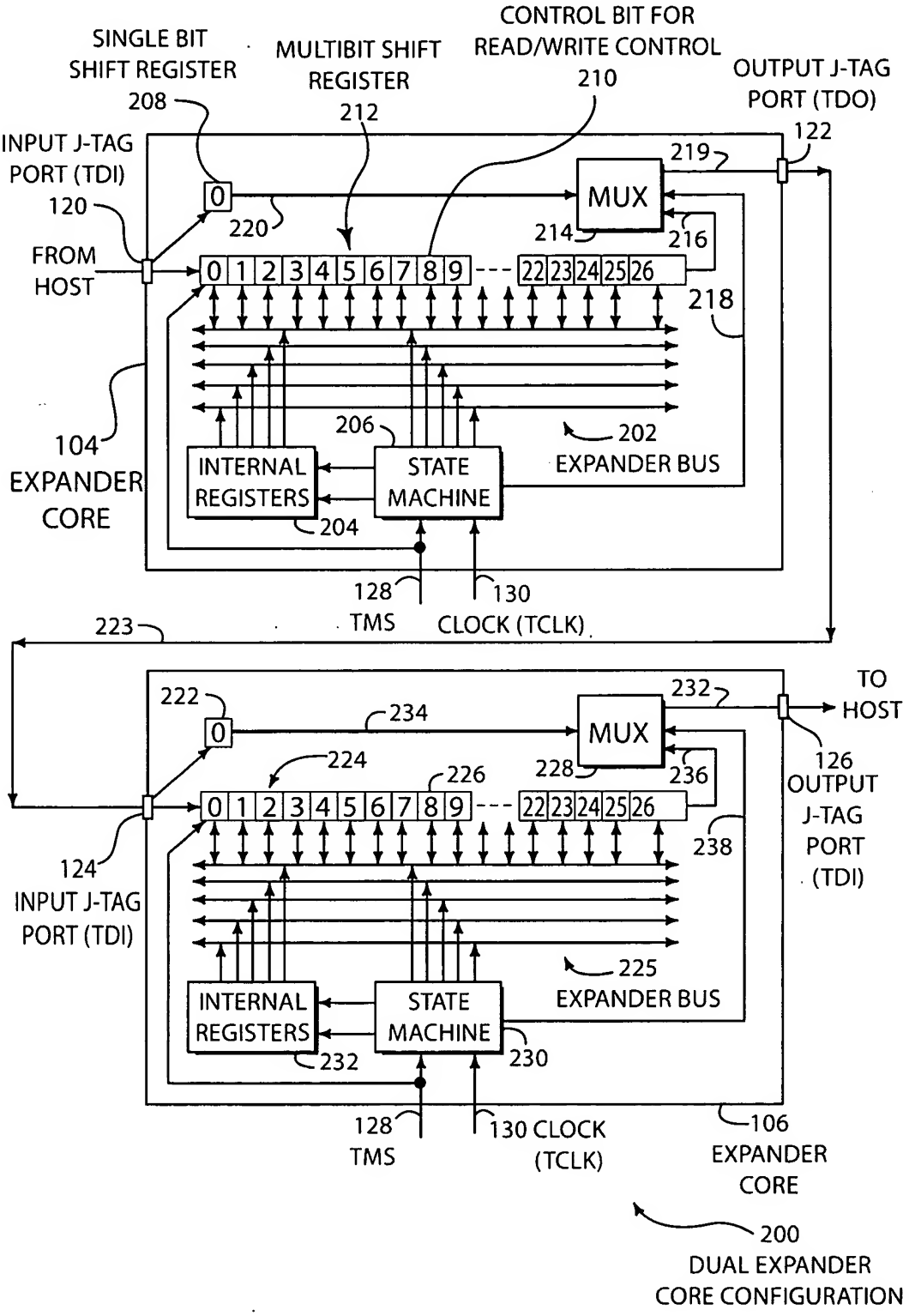
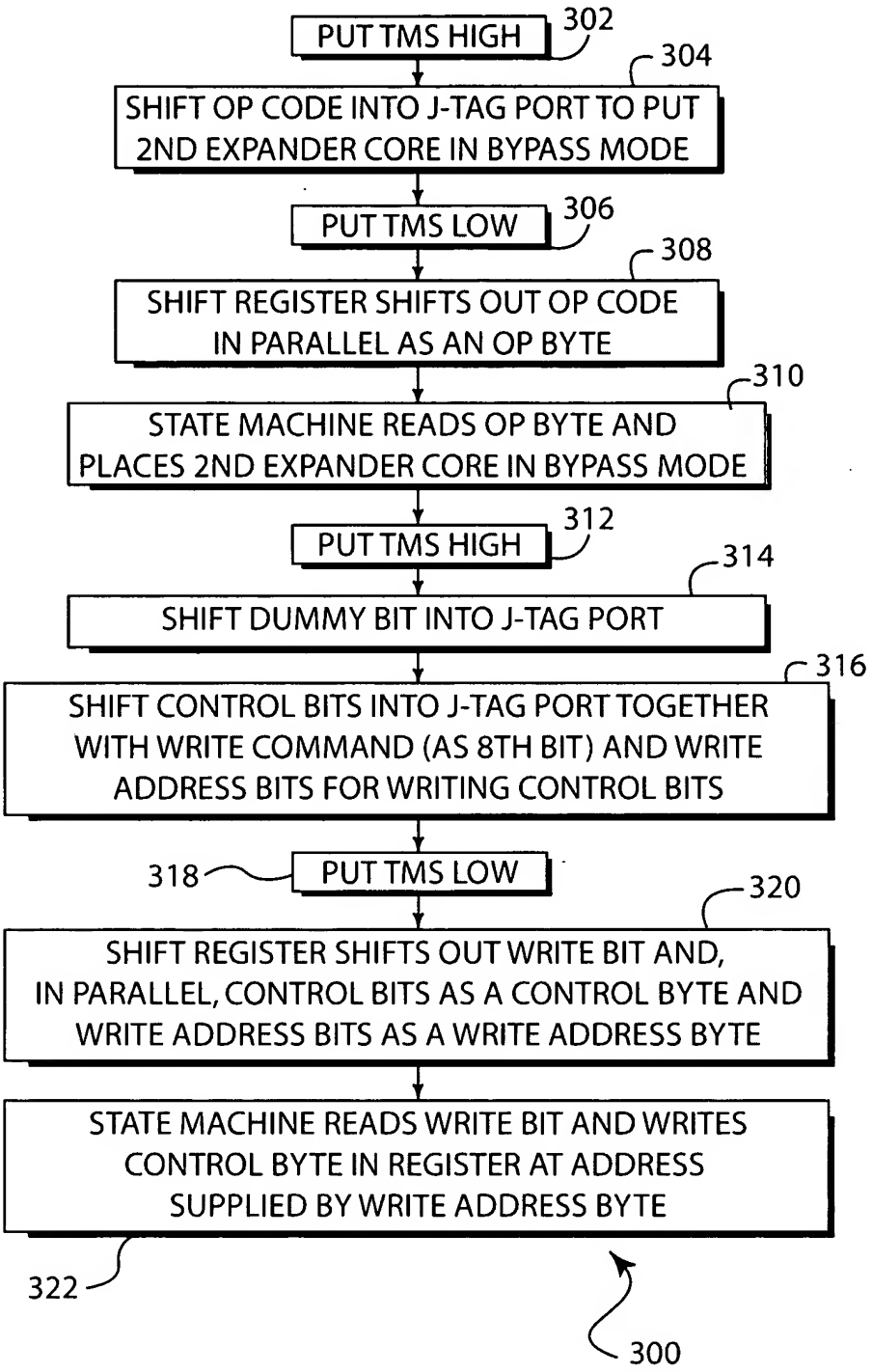
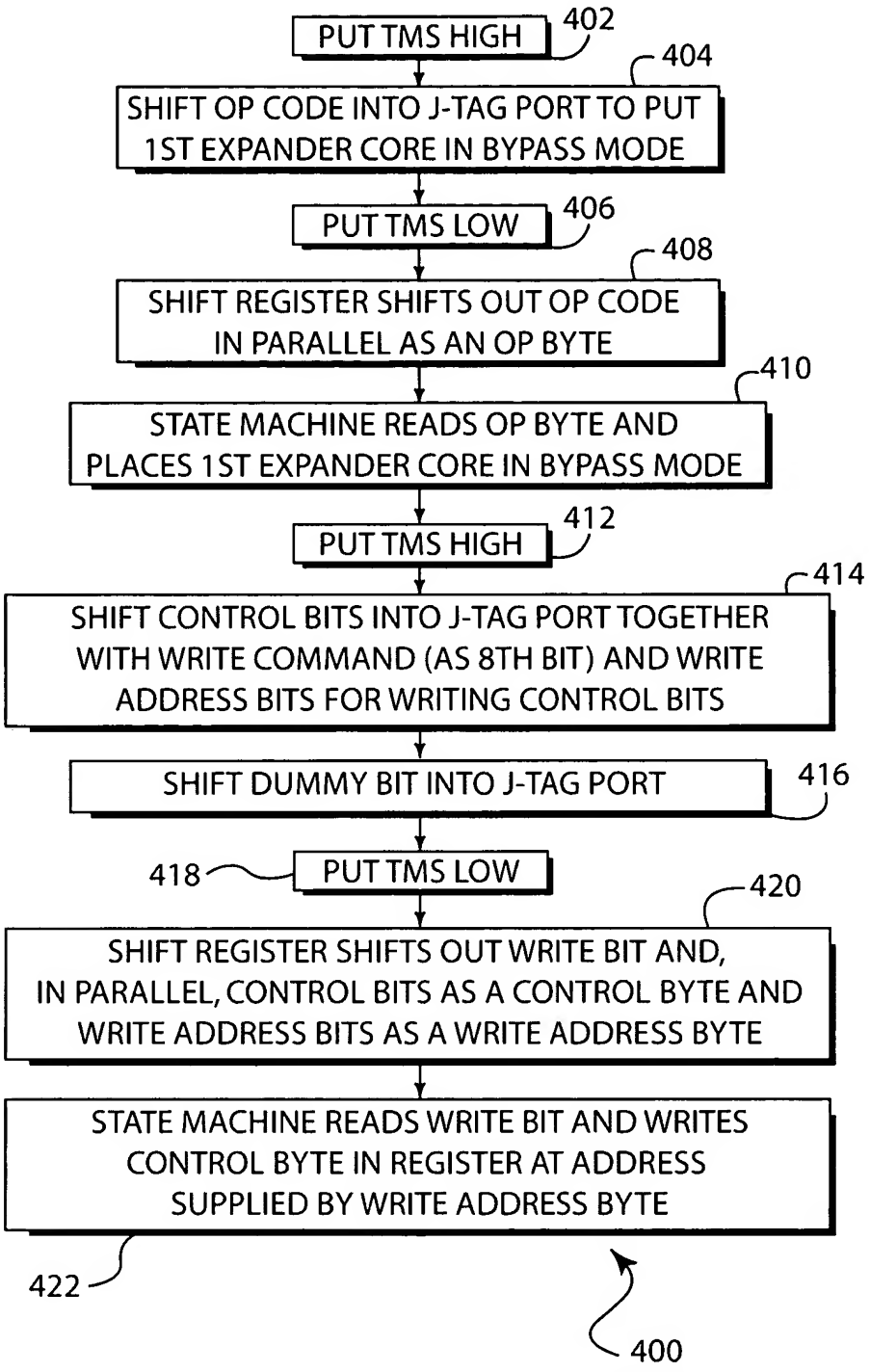


FIGURE 2



PROCESS FOR PERFORMING A REGISTER WRITE OPERATION TO A FIRST EXPANDER CORE

FIGURE 3



PROCESS FOR PERFORMING A REGISTER WRITE OPERATION TO A SECOND EXPANDER CORE

FIGURE 4

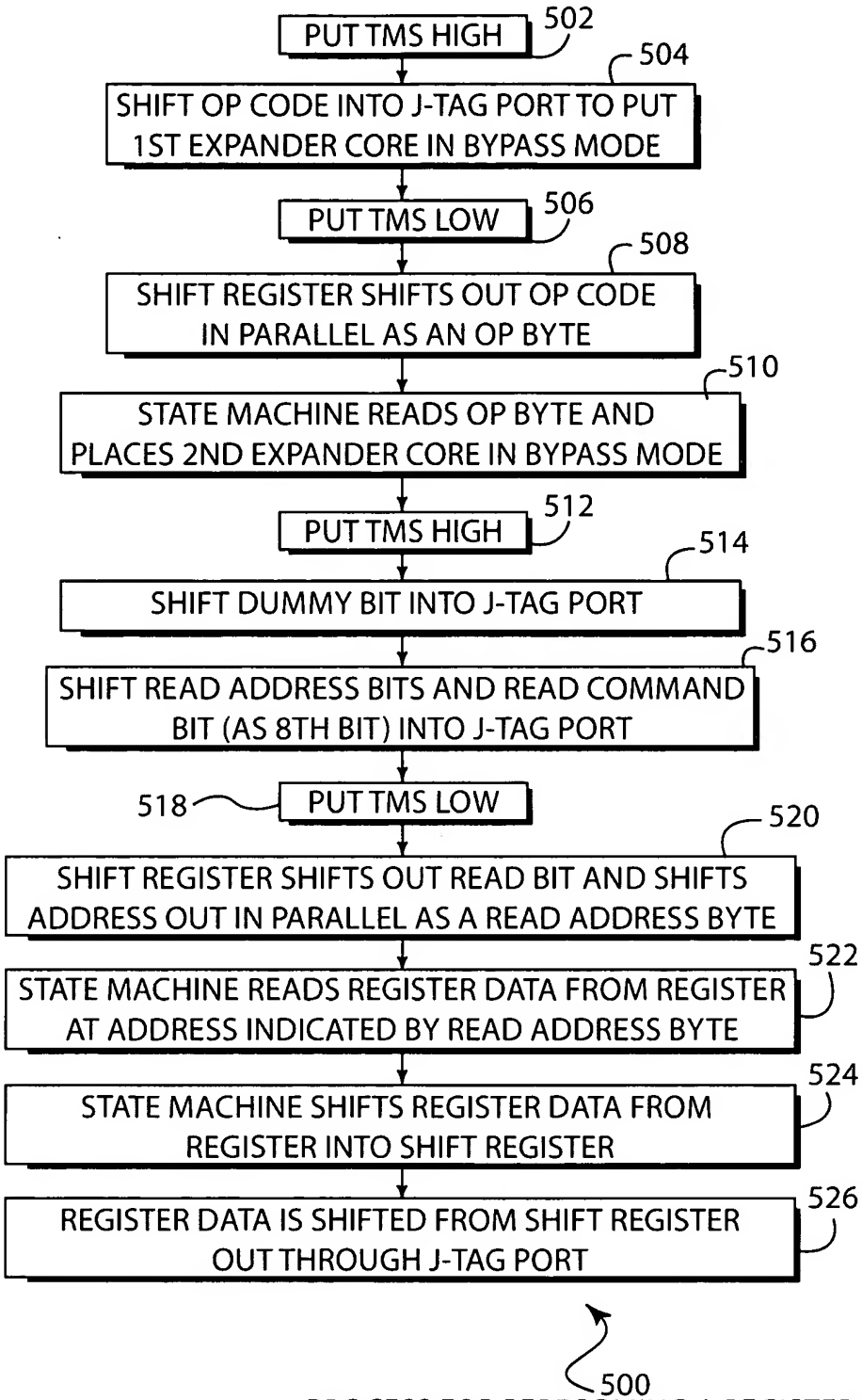

PUT TMS HIGH
502
504
SHIFT OP CODE INTO J-TAG PORT TO PUT 1ST EXPANDER CORE IN BYPASS MODE
PUT TMS LOW
506
508
SHIFT REGISTER SHIFTS OUT OP CODE IN PARALLEL AS AN OP BYTE
510
STATE MACHINE READS OP BYTE AND PLACES 2ND EXPANDER CORE IN BYPASS MODE
PUT TMS HIGH
512
514
SHIFT DUMMY BIT INTO J-TAG PORT
516
SHIFT READ ADDRESS BITS AND READ COMMAND BIT (AS 8TH BIT) INTO J-TAG PORT
518
PUT TMS LOW
520
SHIFT REGISTER SHIFTS OUT READ BIT AND SHIFTS ADDRESS OUT IN PARALLEL AS A READ ADDRESS BYTE
522
STATE MACHINE READS REGISTER DATA FROM REGISTER AT ADDRESS INDICATED BY READ ADDRESS BYTE
524
STATE MACHINE SHIFTS REGISTER DATA FROM REGISTER INTO SHIFT REGISTER
526
REGISTER DATA IS SHIFTED FROM SHIFT REGISTER OUT THROUGH J-TAG PORT
500
PROCESS FOR PERFORMING A REGISTER READ OPERATION FROM A FIRST EXPANDER CORE

FIGURE 5

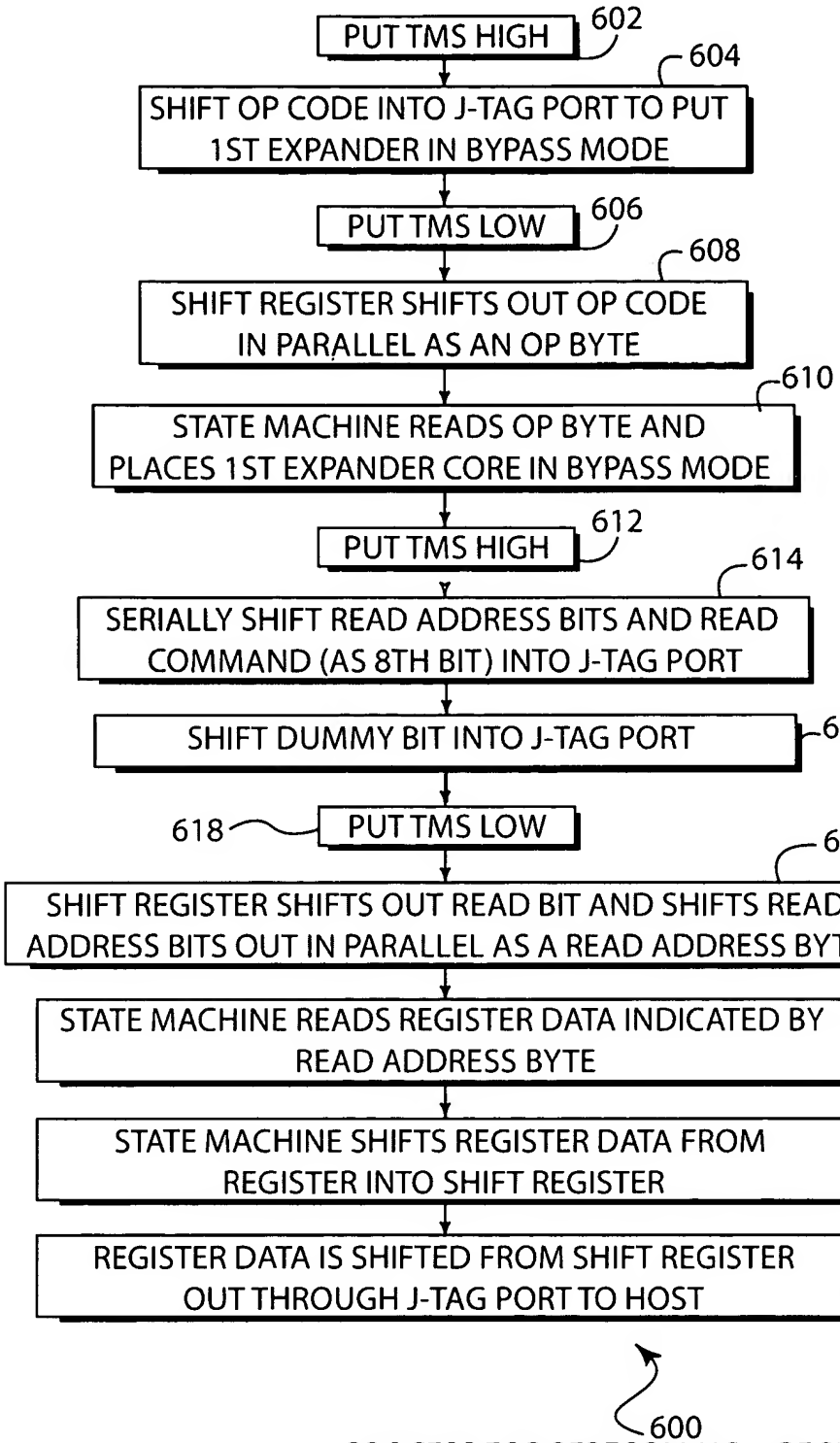

PUT TMS HIGH
602
604
SHIFT OP CODE INTO J-TAG PORT TO PUT 1ST EXPANDER IN BYPASS MODE
PUT TMS LOW
606
608
SHIFT REGISTER SHIFTS OUT OP CODE IN PARALLEL AS AN OP BYTE
610
STATE MACHINE READS OP BYTE AND PLACES 1ST EXPANDER CORE IN BYPASS MODE
PUT TMS HIGH
612
614
SERIALLY SHIFT READ ADDRESS BITS AND READ COMMAND (AS 8TH BIT) INTO J-TAG PORT
SHIFT DUMMY BIT INTO J-TAG PORT
616
618
PUT TMS LOW
620
SHIFT REGISTER SHIFTS OUT READ BIT AND SHIFTS READ ADDRESS BITS OUT IN PARALLEL AS A READ ADDRESS BYTE
STATE MACHINE READS REGISTER DATA INDICATED BY READ ADDRESS BYTE
622
STATE MACHINE SHIFTS REGISTER DATA FROM REGISTER INTO SHIFT REGISTER
624
REGISTER DATA IS SHIFTED FROM SHIFT REGISTER OUT THROUGH J-TAG PORT TO HOST
626
600
PROCESS FOR PERFORMING A REGISTER READ OPERATION FROM A SECOND EXPANDER CORE

FIGURE 6